Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (original) A semiconductor device, comprising:

a test circuit;

a first element; and

a second element comprising at least one of a transmitter and a receiver; wherein when the first element is coupled to the test circuit and the second element is coupled to the first element, at least one of the first and second elements is capable of testing another one of the first and second elements using the test circuit; and

the first element comprises a transmitter when the second element comprises a receiver and the first element comprises a receiver when the second element comprises a transmitter.

2. (original) The semiconductor device of claim 1, wherein the semiconductor device is configured to operate at high frequencies.

3. (original) The semiconductor device of claim 1, wherein the semiconductor device is configured to operate at a frequency of at least 1 Gigahertz.

4. (original) The semiconductor device of claim 1, wherein the semiconductor device is configured to operate at a frequency of at least 3 Gigahertz.

5. (previously presented) The semiconductor device of claim 1, wherein the test circuit includes a pattern generator and a pattern compare circuit.

6. (previously presented) The semiconductor device of claim 1, wherein the semiconductor device is configured to be coupled to at least one reference signal line that carries a voltage reference signal and wherein the test circuit includes at least one comparator circuit to compare at least one voltage signal representing received data with the voltage reference signal.

7. (previously presented) The semiconductor device of claim 6, wherein the at least one reference signal line further carries a time reference signal and the test circuit includes at least one

analog sampling circuit controlled by the time reference signal, wherein the analog sampling circuit receives at least one voltage signal representing received data, such that the time reference signal determines a time offset between receipt of the at least one voltage signal by the receiver and evaluation of the at least one voltage signal by the receiver.

8. (previously presented) The semiconductor device of claim 7, wherein the time reference signal is scannable so as to characterize an actual output eye of the transmitter.

9. (previously presented) The semiconductor device of claim 7, wherein the time reference signal is scannable so as to characterize an actual input eye of the receiver.

10. (currently amended) The semiconductor device of claim 1, wherein the semiconductor device is coupled to an interconnect to receive and transmit a signal representing a complementary voltage value and a signal representing a true voltage value , wherein the test circuit further comprises:

a test pattern generation circuit that generates a plurality of test patterns to be output to a component under test;

a test pattern comparison circuit that compares a test pattern in the plurality of test patterns with a pattern received from the component under test;

a first differential comparator that compares the complementary voltage value with a voltage reference value to output a first result;

a second differential comparator that compares true voltage value with the voltage reference value to output a second result; and

a multiplexer that selects one of the first result and the second result to output to the test pattern comparison circuit. ~~circuit .~~

11. (previously presented) The semiconductor device of claim 10, wherein the test circuit further comprises an analog sampling circuit that delays the signals representing a complementary voltage value and a true voltage value under control of a time reference signal so as to decouple parameters of the transmitter and the receiver.

12. (currently amended) The semiconductor device of claim 11, wherein the delayed signals representing a complementary voltage value and a true voltage value produce a third result, and wherein the multiplexer further selects one of the first result, the second result, and the third result to output to the test comparison circuit. ~~circuit .~~

13. (original) The semiconductor device of claim 12, wherein the transmitter is coupled to the receiver via an interconnect, and wherein the transmitter and the receiver are on a semiconductor wafer.

14. (original) The semiconductor device of claim 12, wherein the transmitter is coupled to the receiver via an interconnect, wherein the interconnect is in a system and is used for system communication between the transmitter and the receiver.

15.-181. (cancelled)